04-06-00

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Washington, DC 20231

Attorney Docket: 1532P
PATENT

Sir:

Transmitted herewith for filing is the Patent Application of

Inventors: **Hung-Mao Lin; Jyh-Cherng Lin; Douglas Chen**

For: **METHOD AND SYSTEM FOR INCREASING YIELD IN EMBEDDED MEMORY DEVICES**

Enclosed with the Patent Application are:

- X Two (2) sheets of informal drawings
- X Declaration of Inventor(s)
- X Power of Attorney by Assignee
- X Declaration Claiming Small Entity Status
- X Assignment and Recordation Form
- __ Information Disclosure Statement (PTO Form 1449)
- X Self Addressed, Stamped Postcard

The filing fee has been calculated as shown below:

	SMALL ENTITY (Col. 1)	(Col. 2)			
FOR:	NO. FILED	NO. EXTRA	RATE		FEE
BASIC FEE					$ 345.00
TOTAL CLAIMS	**20** - 20	= **0**	x 9	=	$ 0.00
INDEP. CLAIMS	**3** - 3	= **0**	x 39	=	$ 0.00
MULTIPLE DEPENDENT CLAIM PRESENTED			+	=	$ 0.00
*If the difference in Col. 1 is less than "0", enter "0" in Col.			**TOTAL**		**$ 345.00**

X Enclosed is check no. 1114 in the amount of **$345.00** for payment of filing fees. A duplicate of this sheet is attached.

Respectfully submitted,

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EXPRESS MAIL CERTIFICATE

I hereby certify that the above paper/fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated below and is addressed to the Commissioner of Patents and Trademarks, Washington, DC 20231. "Express Mail" no.: **EL547854805US**. Date of Deposit: April 4, 2000. Signature of Person mailing paper or fee:

Joseph A. Sawyer, Jr.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: **Hung-Mao Lin; Jyh-Cherng Lin; Douglas Chen**

Title: **METHOD AND SYSTEM FOR INCREASING YIELD IN EMBEDDED MEMORY DEVICES**

POWER OF ATTORNEY BY ASSIGNEE AND EXCLUSION OF INVENTOR UNDER 37 C.F.R. SEC. 1.32

Box Patent Application
Washington, D.C. 20231

Sir:

SILICON MAGIC CORPORATION, INC., a California Corporation, having become the owner of all rights in and to the above-identified application by virtue of an Assignment executed by the inventor concurrently with the execution of the application, said Assignment being submitted herewith for recording, hereby appoints:

JOSEPH A. SAWYER, JR., Reg. No. 30,801
JANYCE R. MITCHELL, Reg. No. 40,095
STEPHEN G. SULLIVAN, Reg. No. 38,329
MICHELE LIU, Reg. No. 44,875
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as their attorneys, to prosecute said application and to transact in connection therewith all business in the Patent and Trademark Office and before competent International Authorities; said appointment to be to the exclusion of the inventor and his attorneys in accordance with the provisions of 37 C.F.R. 1.32:

Date: 3/3/00

Signature: Ray Campbell
Raymond Campbell
Chief Financial Officer

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
)
Lin, et al.)
)
Serial No.)
)
Filed: Herewith)
)
For: **METHOD AND SYSTEM FOR INCREASING YIELD IN EMBEDDED MEMORY DEVICES**)

DECLARATION CLAIMING SMALL ENTITY STATUS UNDER 37 CFR 1.9(f) and 1.27(c) SMALL BUSINESS CONCERN

I hereby declare that I am

[ ] the owner of the small business concern identified below:
[**X**] an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN	**SILICON MAGIC CORPORATION**
ADDRESS OF CONCERN	**920 Stewart Drive**
	Sunnyvale, California 94086-3912

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal years, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention entitled **METHOD AND SYSTEM FOR INCREASING YIELD IN EMBEDDED MEMORY DEVICES** by inventor(s) Hung-Mao Lin, Jyh-Cherng Lin and Douglas Chen, described in the application filed herewith.

The rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this declaration is directed.

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TITLE OF PERSON OTHER THAN OWNER:	**Chief Financial Officer**
ADDRESS OF PERSON SIGNING:	**920 Stewart Drive** **Sunnyvale, California 94086-3912**

Ray Campbell
Signature

3/3/00
Date

UNITED STATES PATENT APPLICATION

FOR

METHOD AND SYSTEM FOR INCREASING YIELD IN EMBEDDED MEMORY DEVICES

Inventor(s):
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METHOD AND SYSTEM FOR INCREASING YIELD IN EMBEDDED MEMORY DEVICES

FIELD OF THE INVENTION

The present invention relates to embedded memory devices, and more particularly to increasing the yield of embedded memory devices.

BACKGROUND OF THE INVENTION

As central processing units for computer systems have undergone constant improvement, computer systems have continued to increase the number of bits they support and their processing speeds. Matching the improvement in other computer system components can be difficult. Included in these components is a semiconductor memory component, such as random access memory (RAM) for the computer system.

Usual attempts to improve the RAM of a computer system involve increases in the amount of RAM in the system. Developers attempt to provide a maximum amount of RAM with minimum area consumption. The decrease in transistor size has allowed greater capacity in RAM circuits. However, area does increase, which causes the percentage of natural good die per wafer to decrease. Thus, the ability to compensate for defective portions of a die becomes more important.

Memory chips typically employ redundancy to supply spare rows/columns of memory cells on the die. The redundant row/columns suitably aid in maintaining higher capacity and compensate for processing defects in the die by replacing defective rows/columns. In order to implement the use of the redundant row/columns, the chip is usually programmed with fuses to select the redundant row/column in place of the defective row/column. However, even the redundant

row/columns may be defective.

Embedded memory devices are particularly concerned with maintaining a high yield of usable memory cells/bits. Embedded memory devices are complex semiconductor circuits that contain both a significant amount of memory and logic cells. After memory repair, if the embedded memory device still exhibits bit locations that are stuck at a one or zero level, the entire embedded memory device becomes unusable. A re-mapping of the failed memory bits is sometimes employed, which consolidates the usable memory cells into one continuous memory space. While re-mapping does allow use of the embedded memory device, the usable memory size is reduced, with one entire row or column discarded for only one failed memory bit.

Accordingly, a need exists for a technique of increasing yield in embedded memory devices.

SUMMARY OF THE INVENTION

The present invention meets this need and provides aspects for increasing yield in an embedded memory device. With the aspects of the present invention, a cache is provided for a memory unit of an embedded memory device. Attempts to access a failed bit memory location in the memory unit are determined. When a failed memory bit location is being accessed, substitution of a memory location in the cache for the failed bit memory location occurs.

With the present invention, an efficient approach to increasing embedded memory device yield is provided. The provision of a cache to substitute for failed memory locations in a memory portion of the embedded memory device allows utilization of memory space substantially equivalent to the intended size of the memory portion. In this manner, the number of usable memory bit locations or yield of the memory portion is increased over prior art approaches of memory re-mapping. Further, the ability to maintain utilization of an embedded memory device

with failed bit locations increases production yield, since fewer devices would need to be discarded. These and other advantages of the present invention will be more fully understood in a conjunction with the following detailed description and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates an example environment of a graphics accelerator in block diagram form within which embedded memory is utilized.

Figure 2 illustrates the embedded memory of Fig. 1 in greater detail with a cache in accordance with the aspects of the present invention.

Figure 3 illustrates a block flow diagram of a method for increasing yield in an embedded memory device in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention relates to increasing yield in an embedded memory device. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

An internal view of a graphics accelerator is illustrated in block diagram form in Figure 1. The graphics accelerator of Figure 1 presents an exemplary device within which embedded memory with increased yield in accordance with the present invention is provided. Of course, the graphics

accelerator serves as just one example of a suitable environment for employing the aspects of the present invention. The architecture includes a host interface 50, a standard VGA module 52, a zoom video port 54, a ROM port 56, four modules of high performance embedded memory 58 (e.g., 1 MB (megabyte) DRAM modules) with increased yield in accordance with the present invention, a two-dimensional engine (2D engine) 60, a three-dimensional engine (3D engine) 62, a motion compensation module 64 for accelerating MPEG-2 playback, and dual display circuitry 66 to support single/simultaneous/dual display on any LCD panel/CRT monitor/TV combination.

One module of the four embedded memory modules 58 is illustrated in more detail in Figure 2. The module 58 suitably includes read and write buffers for the 2D engine 60 and 3D engine 62, namely 3D read buffer 70, 3D write buffer 72, 2D read buffer 74, and 2D write buffer 76. A texture cache 78 is also included for use with the texture data being processed by the graphics accelerator. The module 58 further includes memory unit 80. In accordance with the present invention, the module 58 includes a bad bit cache 82 that is utilized through the control of a memory control unit 84 to increase yield in the embedded memory module 58, as described in more detail hereinbelow with reference to Figure 3.

Referring to Figure 3, a method for increasing yield in an embedded memory device in accordance with the present invention initiates with a performance of a pre-scan operation to identify bad bit locations in the memory unit 80 (step 100). Pre-scan operations are well-known software support programming that occur each time a system is powered on to locate bad bits for identification in the memory control unit 84. Once located, the bad bit locations are preferably stored in a look-up table in the bad bit cache 82 (step 102). The memory control unit 84 then utilizes the look-up table for comparison when access attempts are made to the memory unit 80 in order to determine whether an access being made is to a bad bit location in the memory unit 80

(step 104). When accessing a non-failed memory location, access occurs as is standard to the memory unit 80 (step 106). However, when an access is being made to a failed memory bit location, the memory control unit 84 substitutes a location in the cache for the failed memory bit location and updates the look-up table to associate the cache location with the failed memory bit location (step 108).

Thus, a small cache, such as an SRAM cache, is successfully utilized to replace the failed memory bit(s) in an embedded memory device. The size of one unit of the cache is determined by design needs and may be as small as one byte/8 bits. By way of example, a 64-byte bad bit cache provides suitable support for a 4 MB embedded memory device. Since a cache is considered to provide a higher yield than that of embedded memory, the yield of the embedded memory device is increased with the use of the cache for failed memory bit locations in the memory unit. Further, the cost of the byte-swap technique of using a cache location for a failed embedded memory location in accordance with the present invention is considered to be lower than the cost of row or column repair in the embedded memory device. The use of byte-swapping also allows utilization of memory space substantially equivalent to the entire size of the memory unit, which results in a higher yield of usable memory for the embedded memory device as compared with embedded memory devices re-mapped to compensate for failed memory bits.

Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one or ordinary skill in the art without departing from the spirit and scope of the appended claims.

CLAIMS

What is claimed is:

1. A method for increasing yield of usable memory locations in an embedded memory device, the method comprising:

providing a cache for a memory unit;

determining when an access is made to a failed bit memory location in the memory unit; and

substituting a memory location in the cache for the failed bit memory location when the failed memory bit location is accessed.

2. The method of claim 1 wherein determining when an access is made further comprises identifying each failed bit location in the memory unit and storing each failed bit location in the cache.

3. The method of claim 2 wherein storing further comprises storing each failed bit location in a look-up table.

4. The method of claim 3 wherein determining further comprises comparing a memory location being accessed to identified failed bit locations.

5. The method of claim 2 wherein identifying each failed bit location further comprises performing a pre-scan operation on the memory unit.

6. The method of claim 1 wherein providing a cache further comprises providing an SRAM.

7. The method of claim 1 wherein the memory unit further comprises a DRAM unit.

8. A method for increasing yield of usable memory locations in an embedded memory device, the method comprising:

performing a memory pre-scan operation on an embedded memory device to identify each failed bit location in the embedded memory device; and

swapping a memory location within a cache for a failed bit location.

9. The method of claim 8 further comprising providing the cache between a memory unit and a memory control unit in the embedded memory device.

10. The method of claim 8 further comprising storing each failed bit location in a look-up table in the cache.

11. The method of claim 8 wherein swapping a memory location further comprises swapping when an access attempt is made to a failed bit location.

12. The method of claim 11 further comprising swapping by a memory control unit for the embedded memory device.

13. The method of claim 8 wherein the memory unit further comprises a DRAM unit.

14. The method of claim 8 wherein the cache further comprises an SRAM unit.

15. An embedded memory device with increased yield of usable memory locations, the embedded memory device comprising:

a memory unit;

a cache coupled to the memory unit; and

a memory control unit coupled to the memory unit and the cache, the memory control unit determining when an access is made to a failed bit memory location in the memory unit, and substituting a memory location in the cache for the failed bit memory location when the failed memory bit location is accessed.

16. The embedded memory device of claim 15 wherein the memory unit further comprises a DRAM.

17. The embedded memory device of claim 15 wherein the cache further comprises an SRAM.

18. The embedded memory device of claim 15 wherein the memory control unit further identifies each failed bit location in the memory unit and stores each failed bit location in the cache.

19. The embedded memory device of claim 18 wherein the memory control unit further compares a memory location being accessed to the identified failed bit locations.

20. The embedded memory device of claim 15 further comprising an embedded memory module of a graphics accelerator.

ABSTRACT

Aspects for increasing yield in an embedded memory device are described. With the aspects of the present invention, a cache is provided for a memory unit of an embedded memory device. Attempts to access a failed bit memory location in the memory unit are determined. When a failed memory bit location is being accessed, substitution of a memory location in the cache for the failed bit memory location occurs.

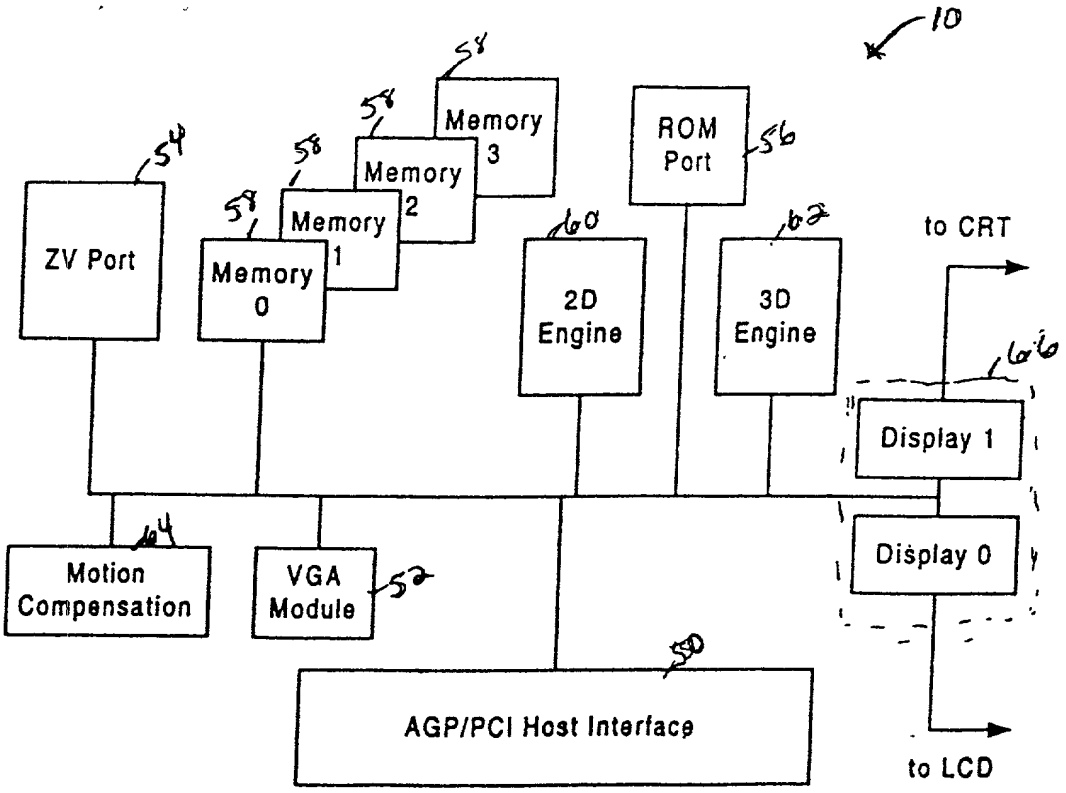

Figure 1

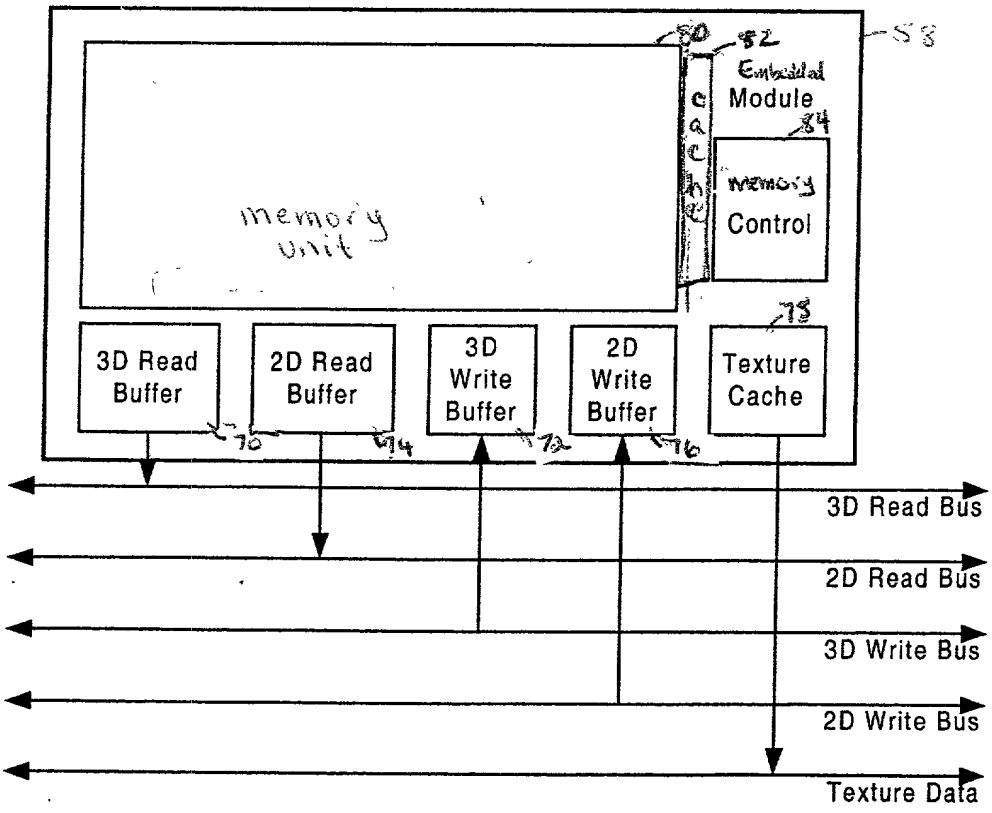

Figure 2

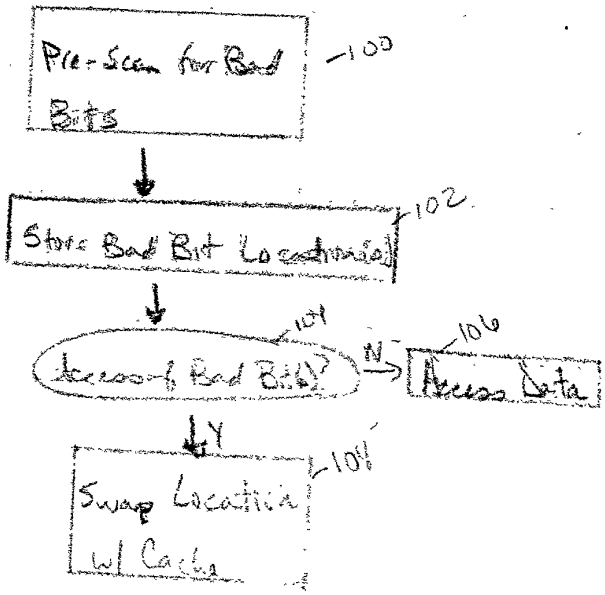
Pre-Scan for Bad Bits
100
Store Bad Bit Location(s)
102
Access Bad Bit(s)?
101
N
Access Data
106
Y
Swap Location w/ Cache
104

Figure 3

DECLARATION

As the below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe I am the original, first and sole inventor of the invention entitled:

METHOD AND SYSTEM FOR INCREASING YIELD IN EMBEDDED MEMORY DEVICES

described and claimed in the specification filed herewith, that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above; that I do not know and do not believe the same was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or legal representatives or assigns more than twelve months prior to this application, that I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application as defined by 37 CFR 1.56, and that no application for patent or inventor's certificate on said invention has been filed in any country foreign to the United States of America by me or my legal representatives or assigns.

Address all telephone calls to Mr. Sawyer at telephone number (650) 493-4540 and all correspondence to:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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